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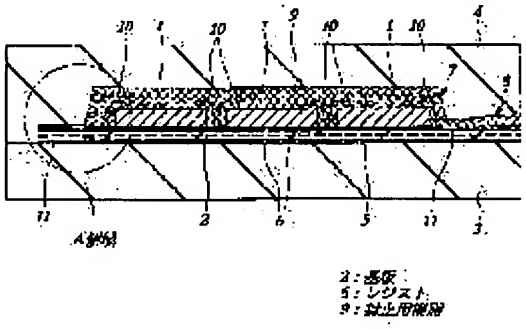
(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide technology for increasing the manufacturing yield of a collectively molded package by preventing the generation of voids on its appearance.

SOLUTION: A region of a resist 6 on a substrate 2 below the entire outer circumference or at least either one side of the outer circumference of a collectively molded sealing resin 9, or a region below the air vent 11 of a molding die is removed by a specified width. Since the region serves as an air vent or a convenient resin reservoir, voids are not trapped easily thus preventing the generation of voids on its appearance.

図 1



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About the manufacturing technology of a semiconductor device, especially this invention is applied to the package mold type CSP (chip size package), and relates to an effective technique.
[0002]
[Description of the Prior Art] After connecting with a leadframe electrically, in order to protect from an external ambient atmosphere or a mechanical shock, the resin seal of the semiconductor chip with which the predetermined integrated circuit was formed is carried out at a mold process. In addition, as an example which has indicated the mold process of a semiconductor device in the detail, there are the Nikkei Business Publications issue, "practice lecture VLSI packaging technical (below)" May 31, 1993 issue, P31-P40, etc., for example.
[0003] As the resin seal approach, shaping of several 10 - about 100 numbers can be performed at once, and a transfer mold with cheap cost is in use. One of the packages to which the closure of the semiconductor chip was carried out by this transfer mold method has the package mold type CSP. A package mold package technique is a technique of manufacturing each semi-conductor product, by carrying out mold by the resin for the closures, and cutting the resin for the closures, and a substrate along a dicing line further, after carrying two or more semiconductor chips of all sizes on a substrate.
[0004]
[Problem(s) to be Solved by the Invention] However, in the above-mentioned package mold package technique, this invention person found out that the following technical problems occurred.
[0005] With a package mold package, depending on the quantity and the chip size of the semiconductor chip carried in a substrate, the distance from a semiconductor chip to a mold edge differs, and the merits and demerits of the distance can amend the restoration time difference of the resin for the closures at the time of mold shaping.
[0006] However, when the above-mentioned distance is remarkable and short, or when a big difference is seen relatively [nature / of the resin for the closures / restoration] in a field with a semiconductor chip, and the field which is not, in order to carry out the trap of the void, without the ability amending the restoration time difference of the resin for the closures, an appearance void may arise and the fall of the manufacture yield of a package mold package will be caused. Although there is the approach of making an air vent deep as a cure in molding metal mold, if it is made deep too much, the problem of resin leakage occurring will arise.
[0007] The purpose of this invention is to offer the technique which can prevent generating of an appearance void and can improve the manufacture yield of a package mold package.
[0008] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0009]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained

among invention indicated in this application.
[0010] The process which prepares the substrate with which this invention was constituted with multilayered wiring, and the resist was applied on the maximum upper wiring, The process which carries two or more semiconductor chips in the front face of a substrate, and shaping metal mold are used. It has the process which covers two or more semiconductor chips and carries out the package mold of the substrate top with the resin for the closures. In advance of the process which carries out the package mold of the substrate top, the resist of all the peripheries of the mold section or a periphery located under any one side or the air vent of shaping metal mold at least is removed with predetermined width of face.
[0011]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.
[0012] (Gestalt 1 of operation) Drawing 1 is the outline sectional view showing an example of the package mold type CSP which is the gestalt 1 of this operation. Drawing 2 is the outline sectional view expanding and showing the area A of drawing 1 . the inside of drawing, and 1 -- a semiconductor chip and 2 -- a substrate and 3 -- the Shimokane mold and 4 -- upper metal mold and 5 -- for a cavity and 8, as for the resin for the closures, and 10, the gate and 9 are [a copper pattern and 6 / a resist and 7 / a wire and 11] air vents.
[0013] The substrate 2 in which two or more semiconductor chips 1 were carried is installed in the Shimokane mold 3, and is being further fixed by the upper metal mold 4. a substrate 2 -- a base substrate -- an insulating layer and a conductor -- the patchboard which formed repeatedly and was multilayered so that wiring might be accumulated by turns, and the so-called build up patchboard can be illustrated. A substrate 2 is about 1mm in thickness, and wiring is constituted by the copper pattern 5. Moreover, in order to protect wiring of the maximum upper layer, the resist (hatching of deep half tone dot meshing shows relatively among drawing) 6 with a thickness of about 20-30 micrometers is applied to both sides of a substrate 2.
[0014] It fills up with the resin 9 for the closures (hatching of thin half tone dot meshing shows relatively among drawing) poured in from the gate 8 in the cavity 7 between the Shimokane mold 3 and the upper metal mold 4, and the closure of the wire 10 which connects a semiconductor chip 1 and a semiconductor chip 1, and the electrode on a substrate 2 is carried out with the resin 9 for the closures. In case the resin 9 for the closures is poured into the upper metal mold 4, the air vent 11 for sending out the air and gas of the resin restoration section in a cavity 7 to the exterior is formed in it, and the depth is about 30-50 micrometers.
[0015] Furthermore, the field located under the periphery of the resin 9 for the closures (the mold section is called hereafter) by which package mold was carried out among the resists 6 on a substrate 2 is removed with predetermined width of face. The above-mentioned field can be made into the field of all the peripheries of the mold section, or a periphery located under any one side or the air vent of shaping metal mold at least. It can make it easy for the field where the resist 6 was removed to achieve the duty of an air vent or a simple resin rich area ball, and to escape the air and gas by which the trap was carried out. Thereby, a void becomes that a trap is hard to be carried out, and can prevent generating of an appearance void.
[0016] Next, an example of the manufacture approach of the package mold type CSP which is the gestalt 1 of this operation is explained in order of a process using drawing 3 - drawing 16 .
[0017] Drawing 3 is the outline perspective view of a substrate, and drawing 4 is the outline sectional view of a substrate. Here, a substrate 2 is prepared. A substrate 2 can illustrate for example, a build up patchboard. Moreover, in both sides of a substrate 2, although the resist 6 with a thickness of about 20-30 micrometers is applied, the resist 6 under all the peripheries of the mold section formed behind is removed with predetermined width of face. in addition, the field where a resist 6 is removed -- the periphery of the mold section -- at least -- the bottom of the air vent of any one side or shaping metal

mold -- you may be .
[0018] Subsequently, drawing 5 is the outline perspective view of the same part as drawing 3 in the continuing production process, and drawing 6 is the outline sectional view of the same part as drawing 4 in the continuing production process. Here, a pellet attachment agent is used for the position on a substrate 2, and two or more semiconductor chips 1 are carried (pellet attachment process).
[0019] Subsequently, drawing 7 is the outline perspective view of the same part as drawing 3 in the continuing production process, and drawing 8 is the outline sectional view of the same part as drawing 4 in the continuing production process. Here, a semiconductor chip 1 and the electrode on a substrate 2 are connected with a wire 10, for example, a gold streak, (wirebonding process).
[0020] Subsequently, drawing 9 is the outline perspective view of the same part as drawing 3 in the continuing production process, and drawing 10 is the outline sectional view of the same part as drawing 4 in the continuing production process. Here, a semiconductor chip 1 and a wire 10 are closed with the resin 9 for the closures (package mold process). For example, package mold is performed as follows.
[0021] First, the upper metal mold of mold equipment is raised and the substrate 2 carrying a semiconductor chip 1 is installed in the Shimokane mold. Then, upper metal mold is lowered and a substrate 2 is fixed. Then, after heating a resin tablet by the pre-heater, and lowering resin viscosity, the resin for the closures is thrown in into shaping metal mold. Then, a blunger is lowered and the resin for the closures is poured in into a cavity through a runner from a pot. Under the present circumstances, since the resist 6 under all the peripheries of the mold section is removed, the air vent of that part becomes large and the air and gas by which the trap was carried out become easy to escape.
[0022] Next, after stiffening the resin for the closures with which it filled up in the cavity by the polymerization reaction, upper metal mold and the Shimokane mold are opened and a substrate 2, a runner, etc. which were covered by the resin for the closures are taken out. Then, the unnecessary resin for the closures is removed and a polymerization reaction is completed by heating at high temperature still more relatively.
[0023] Subsequently, drawing 11 is the outline perspective view of the rear face (field used as the background of the field in which the semiconductor chip 1 was carried) of the substrate in the continuing production process, and drawing 12 is the outline sectional view of the same part as drawing 4 in the continuing production process. Here, the solder ball 12 for connection with a mounting substrate is attached to the rear face of a substrate 2 (ball attachment process).
[0024] Subsequently, drawing 13 is the outline perspective view of the same part as drawing 3 in the continuing production process, and drawing 14 is the outline sectional view of the same part as drawing 4 in the continuing production process. Here, the resin 9 for the closures and a substrate 2 are cut along a dicing line, and each semiconductor device is manufactured (cutting process). Drawing 15 is the outline perspective view of one completed semiconductor device, and drawing 16 is the outline sectional view of one completed semiconductor device.
[0025] Thus, according to the gestalt 1 of this operation, the air and gas by which the trap of it was carried out in the mold process since the field which removed the resist 6 on the substrate 2 of all the peripheries of the mold section or a periphery located under any one side or the air vent of shaping metal mold at least achieved the duty of an air vent or a simple resin rich area ball become easy to escape. Thereby, a void becomes that a trap is hard to be carried out, and can prevent generating of an appearance void.
[0026] (Gestalt 2 of operation) Drawing 17 is the outline sectional view expanding and showing some package mold types CSP which are the gestalten 2 of this operation.
[0027] the conductor constituted by the substrate 2 with the copper pattern 5 like the gestalt 1 of said the operation of this -- wiring is formed, and in order to protect wiring of the maximum upper layer, the resist 6 with a thickness of about 20-30 micrometers is applied to both sides of a substrate 2. Furthermore, it fills up with the resin 9 for the closures in the cavity between the Shimokane mold 3 and the upper metal mold 4, and the closure of a semiconductor chip 1 and the wire 10 is carried out with the resin 9 for the closures. The air vent 11 with a depth of about 30-50 micrometers is formed in the upper metal mold 4.

[0028] However, the predetermined copper pattern 5 of all the peripheries of mold or a periphery located under any one side or the air vent of shaping metal mold at least is removed among the maximum upper wiring of the front face of the substrate 2 in which the semiconductor chip 1 was carried. It can make it easy for the field where the copper pattern 5 was removed to achieve the duty of an air vent or a simple resin rich area ball, and to escape the air and gas by which the trap was carried out. Thereby, a void becomes that a trap is hard to be carried out, and can prevent generating of an appearance void.
[0029] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.
[0030] For example, although the package mold type CSP was mentioned with the gestalt of said operation as a product by which mold is carried out, other substrates are applicable to mold articles, such as what kind of semi-conductor product which carries out mold, for example, LGA (land grid array), BGA (ball grid array), etc., etc.
[0031]
[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
[0032] Since a void becomes that a trap is hard to be carried out and can prevent generating of an appearance void by removing the resist on the substrate of all the peripheries of the mold section, or a periphery located under any one side or the air vent of shaping metal mold at least, or the maximum upper wiring, and forming the field which achieves the duty of an air vent or a simple resin rich area ball, the manufacture yield of a package mold package can be improved.

[Translation done.]

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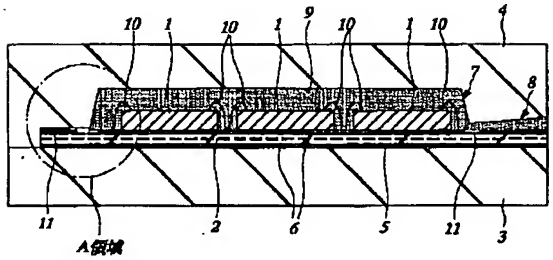
DRAWINGS

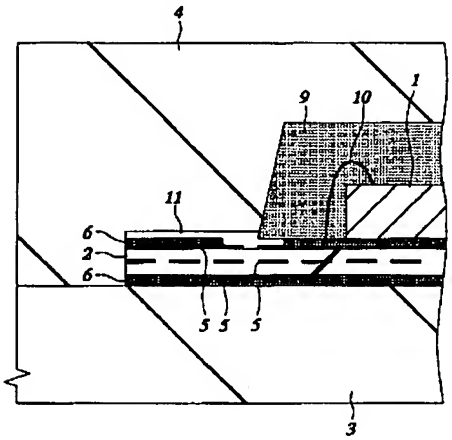
[Drawing 1]

図 1



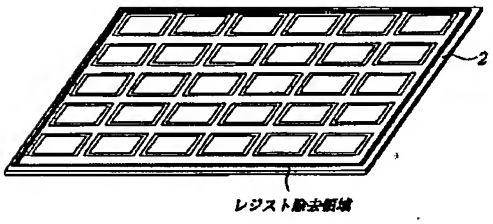
[Drawing 2]

図 2



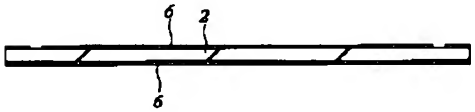
[Drawing 3]

図 3



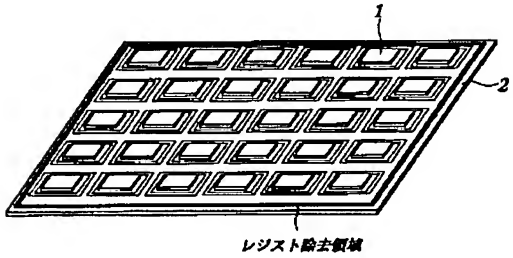
[Drawing 4]

図 4



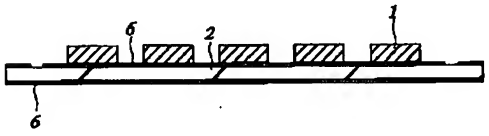
[Drawing 5]

図 5



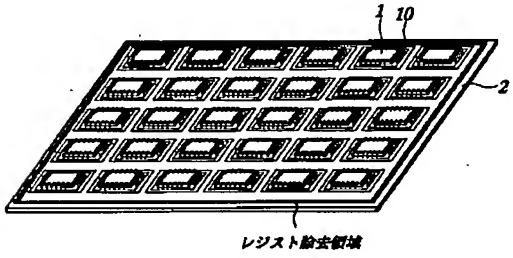
[Drawing 6]

図 6



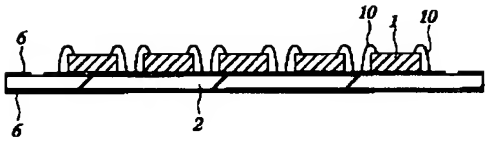
[Drawing 7]

図 7



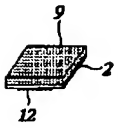
[Drawing 8]

図 8



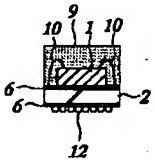
[Drawing 15]

図 15



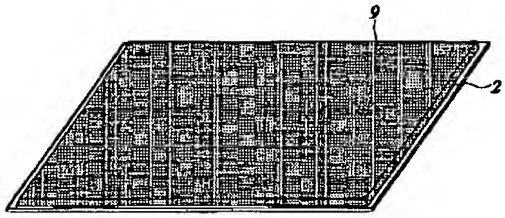
[Drawing 16]

図 16



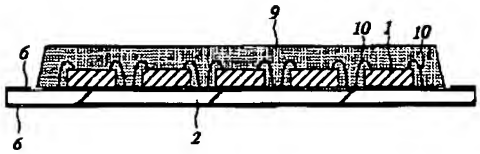
[Drawing 9]

図 9



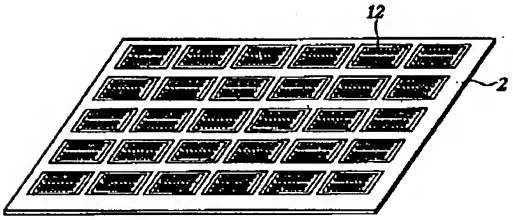
[Drawing 10]

図 10



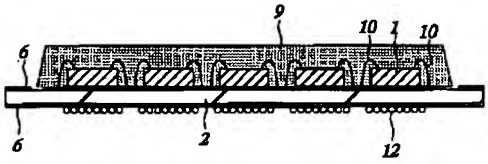
[Drawing 11]

図 11



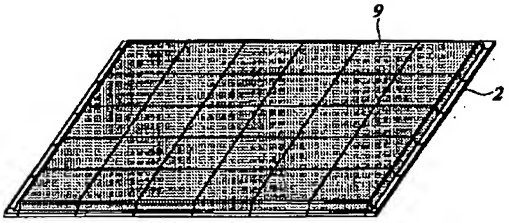
[Drawing 12]

図 12



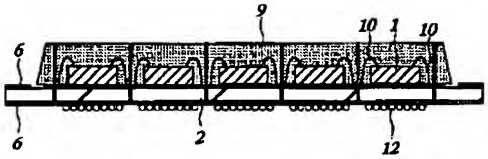
[Drawing 13]

図 13



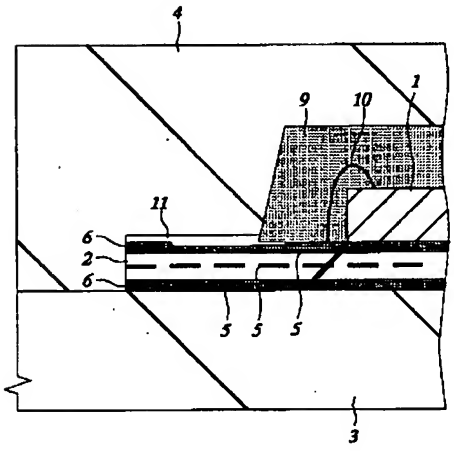
[Drawing 14]

図 14



[Drawing 17]

図 17



[Translation done.]